CLAIMS

1. An apparatus for converting signals of a first preselected voltage level to a second preselected voltage level, comprising:

a transistor having an enable terminal, an input terminal, and an an output terminaland being adapted to receive said signals of the first preselected voltage level, and deliver said signals of the second preselected voltage level;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion adapted to be coupled to a voltage supply.

2. An apparatus, as set forth in claim 1, including a buffer circuit having an input terminal coupled to receive said signals of the second preselected voltage.

3. An apparatus, as set forth in claim 2, wherein said buffer circuit includes an inverter.

4. An apparatus, as set forth in claim 3, including a pull-up transistor adapted to be coupled between the input of said inverter and a voltage supply, and having an enable terminal coupled to the output of said inverter.

5. An apparatus, as set forth in claim 4, wherein said pull-up transistor comprises a PMOS-type transistor.

6. An apparatus, as set forth in claim 1, wherein said resistive element comprises a resistor.

7. An apparatus, as set forth in claim 1, wherein said resistive element comprises an active transistor.

8. An apparatus for converting an input signal of a first preselected voltage level to a second preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain and being adapted to receive said signals of the first preselected voltage level, and deliver said signals of the second preselected voltage level, said gate being adapted to be coupled to a voltage supply having a third preselected voltage level;

a capacitor coupled across said source and drain of said pass gate transistor; and

a pump coupled to the gate of said pass gate transistor, said pump being adapted to temporarily increase the voltage level applied to said gate.

9. An apparatus, as set forth in claim 8, wherein said pump includes a resistive element adapted to be coupled between the gate of said pass gate transistor and said voltage supply, and a capacitor coupled to the gate of said pass gate transistor and being adapted to receive said input signal.

10. An apparatus, as set forth in claim 9, wherein said capacitor coupled to the gate of said pass gate transistor is a parasitic capacitor.

11. An apparatus, as set forth in claim 9, wherein said resistive element is a resistor.

12. An apparatus, as set forth in claim 9, wherein said resistive element is an active transistor.

13. An apparatus for converting an input signal of a first preselected voltage level to a second preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain and being adapted to receive said signals of the first preselected voltage level, and deliver said signals of the second

preselected voltage level, said gate being coupled to a voltage supply having a third preselected voltage level;

a capacitor coupled across said source and drain of said pass gate transistor; and

means for temporarily increasing the voltage level applied to said gate.

14. An apparatus, as set forth in claim 13, wherein said means includes means for increasing the voltage level applied to said gate for a preselected period of time during a transition in said input signal from a logically low voltage level to a logically high voltage level.

15. A method for converting an input signal of a first preselected voltage level to a second preselected voltage level, comprising:

charging a gate of a pass gate transistor to a third preselected voltage level to enable the pass gate transistor to pass at least a portion of the voltage level of the input signal to an output node;

charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time, said fourth preselected voltage level being greater than said third preselected level; and

passing at least a portion of any AC component in said input signal to said output node.

16. A method, as set forth in claim 15, wherein charging the gate of the pass gate transistor to a fourth preselected voltage level includes charging the gate of the pass gate transistor to a fourth preselected voltage level for a preselected period of time during a transition in said input signal from a logically low voltage level to a logically high voltage level.